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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,668	11/04/2003	Kenji Kasahara	740756-2657	6475

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,668	KASAHARA, KENJI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed January 27, 2005 has been entered. Claims 1, 6, 7 and 12 have been amended. Claims 13-24 have been added. Claims 1-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (EP. Patent No. 0485233) in view of Kim et al. (U.S. Patent No. 6,100,954) of record.

With respect to claim 1, Yamazaki teaches a semiconductor device substantially as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a source region and a drain region (34) provided in the semiconductor film (33);

a channel region (28) provided in the semiconductor film (33) between the source region and drain region (34); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is higher than an impurity concentration in an interface between the second insulating film (32b) and the channel region (28). (See Fig. 11A).

Thus, Yamazaki is shown to teach all the features of the claim with the exception of explicitly utilizing organic resin for the gate insulating film.

However, Kim teaches a gate insulating film (157) comprises an organic resin is formed between a gate electrode (113) and channel region (119). (See Fig. 13D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate insulating film of Yamazaki utilizing organic resin as taught by Kim to prevent errors in the TFT operation by parasitic capacitance.

With respect to claim 7, Yamazaki teaches a semiconductor device substantially as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a channel region (28) provided in the semiconductor film (33); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is higher than an impurity concentration in an interface between the second insulating film (32b) and the channel region (28). (See Fig. 11A).

Thus, Yamazaki is shown to teach all the features of the claim with the exception of explicitly utilizing organic resin for the gate insulating film.

However, Kim teaches a gate insulating film (157) comprises an organic resin is formed between a gate electrode (113) and channel region (119). (See Fig. 13D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate insulating film of Yamazaki utilizing organic resin as taught by Kim to prevent errors in the TFT operation by parasitic capacitance.

With respect to claims 2 and 8, semiconductor device of Yamazaki is capable of incorporated into one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a cellular phone, and an electronic book, as claimed.

With respect to claims 3 and 9, the semiconductor film (33) of Yamazaki comprises a material selected from the group consisting of silicon and Si_xGe_{1-x}.

With respect to claims 4 and 10, the semiconductor film (33) of Yamazaki comprises crystalline semiconductor.

With respect to claims 5 and 11, the substrate (11) of Yamazaki is selected from the group consisting of an insulating substrate.

With respect to claims 6 and 12, the organic resin (157) of Kim comprises benzocyclobutene (BCB).

With respect to claims 13 and 15, the second insulating film (32b) of Yamazaki comprises a material selected from the group consisting of silicon oxide.

With respect to claims 14 and 16, the first insulating film (32a) of Yamazaki comprises a material selected from the group consisting of silicon oxide.

3. Claims 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki '233, in view of Yamazaki (JP. Patent No. 06-296,023) and Kim '954.

With respect to claim 17, Yamazaki '233 teaches a semiconductor device substantially as claimed including:

a substrate (11);

a first insulating film (32a) provided over the substrate (11);

a second insulating film (32b) provided over the first insulating film (32a);

a semiconductor film (33) provided over the second insulating film (32b);

a channel region (28) provided in the semiconductor film (33); and

a gate electrode (40) provided over the channel region (28) with a gate insulating film (35) therebetween,

wherein an impurity concentration in an interface between said first insulating film (32a) and the second insulating film (32b) is higher than an impurity concentration

in an interface between the second insulating film (32b) and the channel region (28). (See Fig. 11A).

Thus, Yamazaki '233 is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the first and second insulating film and utilizing organic resin for the gate insulating film.

However, Yamazaki '023 teaches form the first and second insulating film over the substrate such that the second insulating film is thinner than the first insulating film to prevent contaminant out diffusion from the substrate.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second insulating film of Yamazaki '233 to be thinner than the first insulating film as taught by Yamazaki '023 to prevent contaminant out diffusion from the substrate.

Further, Kim teaches a gate insulating film (157) comprises an organic resin is formed between a gate electrode (113) and channel region (119). (See Fig. 13D).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate insulating film of Yamazaki utilizing organic resin as taught by Kim to prevent errors in the TFT operation by parasitic capacitance.

With respect to claim 18, semiconductor device of Yamazaki '233 is capable of incorporated into one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player using a recording medium, a digital camera, a cellular phone, and an electronic book, as claimed.

With respect to claim 19, the semiconductor film (33) of Yamazaki '233 comprises a material selected from the group consisting of silicon and Si_xGe_{1-x}.

With respect to claim 20, the semiconductor film (33) of Yamazaki '233 comprises crystalline semiconductor.

With respect to claim 21, the substrate (11) of Yamazaki '233 is selected from the group consisting of an insulating substrate.

With respect to claim 22, the organic resin (157) of Kim comprises benzocyclobutene (BCB).

With respect to claim 23, the second insulating film (32b) of Yamazaki '233 comprises a material selected from the group consisting of silicon oxide.

With respect to claim 24, the first insulating film (32a) of Yamazaki '233 comprises a material selected from the group consisting of silicon oxide.

Response to Arguments

4. Applicant's arguments with respect to all pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER

March 4, 2005